REMARKS

Reconsideration of the above-captioned patent application is respectfully requested in view of the foregoing amendments and the following remarks.

By this Amendment, claims 1 and 9 have been amended. No new matter is added by the foregoing amendments, and these amendments are fully supported by the specification. Claims 1-12 are pending and are submitted for consideration.

Claims 1-12 Rejected Under 35 U.S.C. § 102(e)

Claims 1-12 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Miyawaki et al. (U.S. Patent No. 6,408,100 B2, "Miyawaki"). Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites an MPEG video decoder comprising, among other features, a frame memory having a plurality of banks and connected to the image decoding section, wherein each of said bank stores one picture and the parameters of each layer decoded by said image decoding section by mutually relating the picture and the parameters as a set, wherein the layer includes a sequence layer which has a horizontal size value and a vertical size value, both expressing sizes of an image, as parameters.

Claim 9 recites an MPEG video decoding method comprising, among other features, the step of storing the decoded picture into said frame memory so as to be combined with the parameters of each layer corresponding to the decoded picture as a set, by relating the decoded picture to the parameters of each layer corresponding to the decoded picture, wherein the layer includes a sequence layer which has a horizontal size value and a vertical size value, both expressing sizes of an image, as parameters.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

In making the rejection, the Office Action characterized Miyawaki as allegedly disclosing "an MPEG video decoder comprising an image decoding section (10 of fig. 1) which decodes parameters of each layer and a picture based on an MPEG bit stream ... Miyawaki further [sic] a frame memory (20 of fig. 2) having a plurality of banks, wherein each of said bank stores one picture and the parameters (display parameters, DP) of each layer decoded by said image decoding section by mutually relating the picture and the parameters, wherein the layer includes a sequence layer (col. 1, lines 17-28, e.g. the horizontal and vertical offsets of the frame are considered as the sequence layer)."

Applicants disagree with the Examiner's characterization of Miyawaki and submit that Miyawaki fails to disclose or suggest each and every element recited in claims 1 and 9 of the present application. In particular, it is submitted that the method and device of moving picture decoding of Miyawaki are neither comparable nor analogous to the MPEG video decoder and the method thereof of the present invention.

In an exemplary embodiment of the present invention as shown on page 18, lines 3 to 7 and 12 to 20 of the specification, a decoded picture and parameters of a sequence layer, a GOP layer, and a picture layer respectively for displaying the decoded pictures are stored in each bank of a frame memory, in order to make a correct display in the MPEG bit stream such as a slide show.

In the Office Action, the Examiner regards the horizontal and vertical offsets, disclosed at column 1, lines 17 to 28 in Miyawaki, as the sequence layer. However, if the reference number 10 is regarded as the image decoding section of the present

invention, then Miyawaki's moving picture decoding device 10 merely includes the display parameter synchronous holding circuit 20, the overall control circuit 12, and the display control circuit 25 as disclosed in Figs. 1 and 2. It is submitted that the configuration as shown in Miyawaki fails to disclose the features as exemplified in Fig. 6, for example, of the present invention.

With respect to the present invention of storing one picture and the parameters (display parameter DP) of each layer in a plurality of banks, Miyawaki merely discloses DAT1, which is I-picture, is stored through memory bus 14 and memory control circuit into decoded data area 132 of memory 13 as decoded picture data DAT2, at column 4, lines 18 to 55. Data in area 132 is read out by memory control circuit 11, and is provided through memory bus 14 into display circuit, and display parameters and picture coding type PCT of the control data are provided into display parameter synchronous holding circuit 20, wherein the display parameters corresponding to pictures processed by display circuit 19 are provided into display circuit 19.

As described above, the display parameter synchronous holding circuit 20 of Miyawaki, which the Examiner construes as the frame memory 20, only stores the display parameters, but does not store the decoded picture as claimed in the present invention. In particular, Miyawaki stores the I-picture into the decoded data area 132 of memory 13 as decoded picture data DAT2; and memory 13 of Miyawaki is a different element from the frame memory 20. Therefore, Miyawaki fails to disclose at least the features of the present invention that a decoded picture and parameters of a sequence layer, a GOP layer, and a picture layer respectively for displaying the decoded pictures are stored in each bank of a frame memory.

Furthermore, the Examiner regards Miyawaki's frame center offsets (horizontal and vertical offsets) at column 1 lines 17 to 28 thereof, as the sequence layer of the present invention. As disclosed at page 2, line 23 to page 3 line 16 of the present invention, for example, the sequence layer has a horizontal size value and a vertical size value as parameters. For instance, the sequence layer of the present invention in MPEG includes parameters expressing horizontal and vertical sizes of an image such as H-Size, V-Size, D-H-Size, D-V-Size. Hence, it is submitted that Miyawaki fails to disclose or suggest at least the features of "a frame memory having a plurality of banks and connected to the image decoding section, wherein each of said bank stores one picture and the parameters of each layer decoded by said image decoding section by mutually relating the picture and the parameters as a set, wherein the layer includes a sequence layer which has a horizontal size value and a vertical size value, both expressing sizes of an image, as parameters" and "storing the decoded picture into said frame memory so as to be combined with the parameters of each layer corresponding to the decoded picture as a set, by relating the decoded picture to the parameters of each layer corresponding to the decoded picture, wherein the layer includes a sequence layer which has a horizontal size value and a vertical size value, both expressing sizes of an image, as parameters."

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Miyawaki fails to disclose or suggest each and every feature of claims 1 and 9. Accordingly, Applicants respectfully submit that claims 1 and 9 are not anticipated by nor

rendered obvious by the disclosure of Miyawaki. Therefore, Applicants respectfully submit that claims 1 and 9 are allowable.

As claims 2-8, 10 and 11 depend from claim 1, and claim 12 depends from claim 9, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, Applicants respectfully request withdrawal of the rejection.

CONCLUSION

Applicants respectfully submit that the above-captioned patent application is in condition for allowance, and such action is earnestly solicited.

If the Examiner believes that an in-person or telephonic interview with Applicants' representatives would expedite the prosecution of the above-captioned patent application, the Examiner is invited to contact the undersigned attorney of records. Applicants believe that no fees are due as a result of this response to the outstanding Office Action in the above-captioned patent application.

In the event of any variance between the fees determined by Applicants and those determined by the U.S. Patent and Trademark Office, please charge any such variance to the undersigned's Deposit Account No. 01-2300 referencing docket number 108391-00014.

Respectfully submitted,

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Enclosure: RCE Transmittal w/Fees